LISTING OF THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the present application.

Listing of the Claims:

1. (Currently amended) An active pixel sensor comprising:

a P-well;

a photoreceptor outside said P-well;

an NMOS frame shutter within the P-well, said frame shutter including a first storage area for receiving charges from said photoreceptor, a second storage area for receiving charges from said first storage area, a sample and hold circuit for gating charges from said first storage area to said second storage area, and respective reset circuits for said first and second storage areas; and

an active pixel readout for receiving charges from said second storage area of said NMOS frame shutter.

2. (Cancelled).

3. (Cancelled).

4. (Currently amended) The active pixel sensor of Claim [[3]] 1, wherein the sample and hold and reset circuits comprise NMOS transistors.

5-12. (Cancelled).

13. (Currently amended) An active pixel sensor comprising:

a P-well;

a photoreceptor, wherein the photoreceptor comprises a pinned photodiode;

an NMOS frame shutter within said P-well, said frame shutter including a first storage area for receiving charges from said photoreceptor, a second storage area for receiving charges from said first storage area, and respective reset circuits for said first and second storage areas;

and

an active pixel readout circuit for receiving charges from said NMOS frame shutter.

14. (Currently amended) The active pixel sensor of Claim 13, wherein the frame shutter includes a sample and hold circuit between said first and second storage areas ~~and reset circuits~~, and wherein the pinned photodiode is fabricated within said substrate and outside said P-well.

15. (Original) The active pixel sensor of Claim 14, wherein the sample and hold and reset circuits comprise NMOS transistors.

16-19. (Cancelled).

20. (Currently amended) An active pixel sensor comprising:

a P-well;

a photoreceptor outside said P-well;

an active pixel readout circuit, comprising source follower and row select transistors;

and

an NMOS frame shutter comprising ~~sample and hold and reset circuits~~ a first storage area for receiving charges from said photoreceptor, a second storage area for receiving charges from said first storage area, a sample and hold circuit for gating charges from said first storage area to said second storage area, and respective reset circuits for said first and second storage areas, fabricated within the P-well, wherein the sample and hold circuit is in direct electrical connection to the source follower transistor of the active pixel readout circuit.

21. (Previously presented) The active pixel sensor of Claim 20 wherein the photoreceptor is a pinned photodiode.

22. (Previously presented) The active pixel sensor of Claim 20 wherein the sample and hold and reset circuits are NMOS transistors.

23-24. (Cancelled)

25. (Currently amended) An integrated pixel sensor comprising:

a P-well;

a photoreceptor outside said P-well;

a frame shutter fabricated in said P-well, said frame shutter comprising a first storage node for receiving charges from said photoreceptor ~~and~~ , a transistor for

sampling charges from said ~~photoreceptor~~ first storage node on to ~~said~~ a second storage node, and respective reset circuits for said first and second storage nodes; and

a readout circuit for receiving charges from said second storage node and providing a readout signal.

26. (Previously presented) The integrated pixel sensor of Claim 25, wherein the transistor for sampling charges is an NMOS transistor.

27. (Previously presented) The integrated pixel sensor of Claim 25, wherein the photoreceptor is a pinned photodiode.

28. (Currently amended) An integrated pixel sensor comprising:

a P-well;

a photoreceptor outside said P-well;

a frame shutter fabricated in said P-well, said frame shutter comprising a first storage node for receiving charges from said photoreceptor, a sample and hold circuit for receiving charges from said ~~photoreceptor~~ first storage node and sampling charges from said ~~photoreceptor~~ first storage node on to ~~a~~ second storage node, and second respective reset circuits for said first and second storage nodes; and

a readout circuit for receiving charges from said storage node and providing a readout signal, said readout circuit comprising an active pixel readout circuit in direct electrical connection to said sample circuit.

29. (Previously presented) The integrated pixel sensor of Claim 28, wherein the sample circuit comprises an NMOS transistor for receiving said charges.

30. (Previously presented) The integrated pixel sensor of Claim 28, wherein the photoreceptor is a pinned photodiode.